EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	4	"620470".ap.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/25 17:50
S2	657	vcc1 near10 vcc2	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/26 13:46
S3	8	S2 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/26 13:46
S4	1	"6747855".pn.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/26 13:47
S5	38630	(two dual second multiple many several few couple) near6 (voltage power$3 vcc$) near6 (pins terminals connector$1)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:09
S6	263	S5 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 09:02
S7	18822	S5 same (ic circuit board chip)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 09:02
S8	135	S7 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 09:04
S9	13046	(two dual second multiple many several few couple) adj6 (voltage power$3 vcc$) adj6 (pins terminals connector$1)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 09:04
S10	93	S9 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 09:04
S11	6670	(second another shadow redundant) near6 (power voltage vcc) near6 (pin connector adapter)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 10:12

EAST Search History

S12	376768	(supply$3 maintain$3 provid$3 deliver$3) near6 (mode$1 state$1 sleep low$power)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 10:09
S13	74	S11 near10 S12	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 09:53
S14	2	S13 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 09:53
S15	72	S13 not S14	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 09:55
S16	71060	(supply$3 maintain$3 provid$3 deliver$3) near6 (voltage power) near6 (mode$1 state$1 sleep low$power)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 10:10
S17	8544	(supply$3 maintain$3 provid$3 deliver$3) near6 (voltage power) near6 ((sleep low low$power stand$by) near3 (mode$1 state$1))	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 10:11
S18	10493	(supply$3 maintain$3 provid$3 deliver$3 receiv$3 accept$3) near6 (voltage power) near6 ((sleep low low$power stand$by) near3 (mode$1 state$1))	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 10:12
S19	174322	(second another shadow redundant) near6 (pin connector adapter)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 10:12
S20	3	S18 near10 S19	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 10:14
S21	8	S18 same S19	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 10:14
S22	5	S21 not S20	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 10:14
S23	1	"5530612".PN.	USPAT; USOCR	OR	OFF	2006/10/27 10:44
S24	1	"5561577".PN.	USPAT; USOCR	OR	OFF	2006/10/27 10:48

EAST Search History

S25	1	"5617283".PN.	USPAT; USOCR	OR	OFF	2006/10/27 10:48
S26	1	"5886862".pn.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:05
S27	1180	(ic (integrated adj1 circuit)) near10 ((sleep low$power stand$by) near3 (mode$1 state$1))	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 12:03
S28	36830	(two dual second another couple) near6 (voltage power$3 vdd$ vcc$) near6 (pins terminals connector$1)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:19
S29	4	S27 same S28	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:20
S30	112	S27 and S28	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:11
S31	1	S30 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:11
S32	74475	(two dual second another couple) near6 (voltage power$3 vdd$ vcc$) near6 (pin$1 terminal$1 connector$1)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:19
S33	25	S27 same S32	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:20
S34	21	S33 not S29	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:28
S35	107	vid near6 power	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:43
S36	0	S32 same S35	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:45

S37	12	S32 and S35	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:45
S38	210	(maintain$3 sav$3 retain$3) same S27	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 12:06
S39	13	S28 and S38	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 11:52
S40	2773	(processor$1) near10 ((sleep low$power stand$by) near3 (mode$1 state$1))	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 12:06
S41	7	S32 same S40	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 12:03
S42	315	(processor$1) near10 S32	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 12:06
S43	7554	(maintain$3 sav$3 retain$3) near10 ((sleep low$power stand$by) near3 (mode$1 state$1))	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 12:07
S44	0	S42 same S43	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 12:07
S45	5	S42 and S43	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 12:07
S46	7900	transmission adj1 gate	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 14:11
S47	132450	(between coupl$3 connect$3 rout$3) near6 (pin$1 terminal$1 connect$4) near6 ((power voltage) near3 (regulat$4 supply$3 circuit))	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 14:14
S48	146	S46 near10 S47	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 14:15

S49	1	S48 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 14:15
S50	1799059	ic ics (integrated adj1 circuit$1) circuit$1	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 16:45
S51	1509973	(two dual couple second) near6 (pin$1 terminal$1 connect$4)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 16:47
S52	1705717	(two dual couple second more few) near6 (pin$1 terminal$1 connect$4)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 16:47
S53	671529	(sleep low$power stand$by off operat$4) near3 (state$1 mode$1)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 16:48
S54	15700	S50 same S52 same S53	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/27 16:48
S55	1	"6308278".pn.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 14:33
S56	1	"5375247".pn.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 14:37
S57	543786	(power voltage) near6 (supply regulator)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 15:26
S58	65686	(high adj1 (impedance z)) tri$stat$3	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 15:28
S59	2235	S57 near10 S58	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 15:28
S60	27	S59 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 15:28

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S61	1	"4593349".PN.	USPAT; USOCR	OR	OFF	2006/10/28 16:10
S62	1	"4674031".PN.	USPAT; USOCR	OR	OFF	2006/10/28 16:11
S63	1	"5560022".PN.	USPAT; USOCR	OR	OFF	2006/10/28 16:11
S64	1	"6212645".PN.	USPAT; USOCR	OR	OFF	2006/10/28 16:12
S65	1	"6237103".PN.	USPAT; USOCR	OR	OFF	2006/10/28 16:12
S66	13668	(sav$3 retain$3 back$up mov$3) near10 (ic (integrated adj1 circuit) chip system) near10 (state status)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:43
S67	20526	receiv$3 near6 interrupt$1	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:38
S68	812	S66 and S67	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:38
S69	33	S68 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:38
S70	148	(memory storage) near6 on$die	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:43
S71	161943	(sav$3 retain$3 back$up mov$3) near10 (state status)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:46
S72	56774	(low$power sleep stand$by) near6 (state mode)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:43
S73	5	S70 and S71 and S72	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:44
S74	13668	(sav$3 retain$3 back$up mov$3) near10 (ic (integrated adj1 circuit) chip system) near10 (state status)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:52

S75	1	S70 same S74	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:47
S76	3	S70 and S74	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:47
S77	329162	(sav$3 retain$3 back$up mov$3) near10 (data state status)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:55
S78	2236	S77 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:55
S79	196	S72 and S78	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:55
S80	73	S79 and interrupt	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:56
S81	155638	(sav$3 retain$3 back$up) near10 (data state status)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:55
S82	1319	S81 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 16:55
S83	171	S72 and S82	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 17:00
S84	2945	S72 same S81	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 17:00
S85	60	S84 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:03
S86	114289	(on$die ic (integrated adj1 circuit) chip) near6 (storage memory)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 17:08

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S87	1899	S81 same S86	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 17:08
S88	54	S87 same S72	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/28 17:08
S89	56774	(low$power sleep stand$by) near6 (state mode)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/29 14:27
S90	155638	(sav$3 retain$3 back$up) near10 (data state status)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/29 14:27
S91	2945	S89 same S90	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/29 14:27
S92	60	S91 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/29 14:28
S93	56774	(low$power sleep stand$by) near6 (state mode)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:03
S94	155638	(sav$3 retain$3 back$up) near10 (data state status)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:04
S95	2945	S93 same S94	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:05
S96	461	S95 and 713/300-340.ccls.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:05
S97	430	S96 not intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:06
S98	72876	(sav$3 retain$3 back$up) near10 ((system near2 (information data code)) state status vid)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:05

S99	71309	S98 same S94	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:27
S10 0	1268	S99 and 713/300-340.ccls.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:27
S10 1	75	S100 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:27
S10 2	60	S95 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:23
S10 3	44	S101 not S102	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:24
S10 4	40	S95 and intel.as. and (ic (integrated adj1 circuit) chip die)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:24
S10 5	30	S101 not S102 and (ic (integrated adj1 circuit) chip die)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:28
S10 6	2199	S98 same S93	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:27
S10 7	388	S106 and 713/300-340.ccls.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:27
S10 8	31	S107 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:27
S10 9	17	S108 and (ic (integrated adj1 circuit) chip die)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 08:28
S11 0	53	suspendtoram	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 10:07

EAST Search History

S11 1	13	S110 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 10:07
S11 2	10860	feed$back near10 ((power voltage) near3(regulator supply))	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 11:40
S11 3	102	S112 and intel.as.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 11:40
S11 4	11	S113 and 713/300-340.ccls.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2006/10/30 11:40